**SCL TAPEOUT SUBMISSION FORM THROUGH CHIPIN CENTRE**



SEMICONDUCTOR LABORATORY

SECTOR 72, S.A.S. NAGAR

(NEAR CHANDIGARH)

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This document provides information on various items, which must be considered when a layout is provided to ChipIN Centre, C-DAC Bangalore to fabricate through Semi-Conductor Laboratory (SCL) for processing with 180nm CMOS technology.

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# General Guidelines

Please follow carefully all the guidelines given herein to ensure correct and timely processing of your Designs/Circuits.

* 1. **Data Format and Communication:**
     + Acceptable database format is GDSII only.
     + Complete database must be sent through e-mail to ‘chipin@cdac.in’. Do not provide any google drive link.
     + The communication has to be addressed through mail at:

To: chipin@cdac.in  
CC: venkatark@cdac.in, viviand@cdac.in, support.c2s@meity.gov.in  
ChipIN Centre,   
Chips to Start-up (C2S) Programme,  
C-DAC Bangalore,  
Opp. HAL Aeroengine Division,  
Old Madras Road, Byappanahalli,  
Bengaluru - 560 038.

* 1. **Layout Grid**
     + Minimum grid size used in the GDSII must be integer multiple of 0.005µm.
     + Final GDSII window (including seal ring) must have Bottom left corner at (0,0) coordinate and the Top-Right corner coordinate must be rounded off to closest even number and it should be without any decimal places i.e., 10102 µm or 10100 µm for the case if coordinate comes at 10101.395 µm.
  2. **Design Kit**
     + Do not rename cell names used in cell library.
     + Do not use library cell name for custom designed cells.
     + Do not edit standard cell library and I/O library.
  3. **Design Verification**
     + Customers must provide a clean GDSII database w.r.t. DRC, Density and Antenna rules.
     + Before taping out the data, please provide checksum for GDSII file. Save the checksum value and byte count in a file, so that the same can be crosschecked at our end. e.g. cksum EDU0001\_01012016\_v1.gds 12345678 204 EDU0001\_01012016\_v1.gds
     + For GDSII integrity check while data transfer MD5 checksum is must and need to be provided in addition to checksum so that the same can be crosschecked at our end. For calculating MD5, Just open Linux terminal and type: md5sum ‘filename’ e.g. md5sum SC0001-0E\_25012023\_v1.gds
     + GDSII name and Top cell name format: silicon\_no\_date\_version.gds (date format should be ddmmyyyy) and top cell name should be "silicon number" only.
     + All the reports should be named as GDSII name.

Eg: silicon no\_date\_version\_drc.rpt, silicon no\_date\_version\_drc.summary, silicon no\_date\_version\_ant.rpt etc.

* + - Process Information Sheet (PIS sheet): All the columns must be filled with the drop-in information wherever provided. At places where drop-in is not given, designer must write as per the column description only.

# Product Related Information

1. **Customer Information**

Name of the Organization :

Contact Person & Designation :

Tel./Mob. :

Email :

1. **Project Information**
   1. Product/Design name :
      * Silicon Number (Issued by SCL) :
   2. Brief Description of the circuit :

(Description of the circuit should include Introduction, application, frequency, work flow)

**Please attach separate sheet.**

* 1. Physical Design (layout) EDA Tool name and Version (Please specify) :

* 1. Top cell Name :

Please distinguish between lower- and UPPER-case letters (case sensitive)

* 1. Die coordinates with seal ring (µm) X min: X max:

Y min: Y max:

* 1. Die Size (µm) :
  2. GDSII File Name :
  3. GDSII File Size in bytes :
  4. GDSII Checksum :
  5. GDSII MD5 value :

2.11 **SCL PDK (Name, Version and revision):**

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 2.12 | **Standard cell library:** |  | **fs120** |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |
| 2.13 | **IO library:** |  | **cio150** |  | **cio250** |  | **pio520** |  |
|  |  |  |  |  |  |  |  |  |
| 2.14 | **Metal level:** |  | **4M1L** |  | **6M1L** |  |  |  |
|  |  |  |  |  |  |  |  |  |
|  | **IO voltage:** |  | **1.8V Only** |  | **3.3V Only** |  | **5V Only** |  |
| 2.15 |  |  |  |  |  |  |  |
|  |  | **1.8V & 3.3V** |  | **1.8V & 5V** |  |  |  |
|  |  |  |  |  |  |  |  |  |
|  | **Core voltage:** |  | **1.8V Only** |  | **3.3V Only** |  | **5V Only** |  |
| 2.16 |  |  |  |  |  |  |  |
|  |  | **1.8V & 3.3V** |  | **1.8V & 5V** |  |  |  |
|  |  |  |  |  |  |  |  |  |
| 2.17 | **Mosfets type (core only):** |  | **1.8V** |  | **3.3V** |  | **5V** |  |
|  |  |  |  |  |  |  |  |  |
| 2.18 | **Device Application:** |  |  |  |  |  |  |  |

**Note:** 3.3V and 5V transistors are not allowed in a single design because this is an illegal combination. For more info regarding all such type of allowed and illegal combination, please refer PDK ReadMe.

1. **Tapeout Checklist**

|  |  |
| --- | --- |
| **Device related information** | **Yes/No** |
| GDSII database provided |  |
| Silicon Number with PCI is mandatory. GDSII for this is included in the PDK.  (Layer revision block may be placed if space permit) ? |  |
| Seal Ring with GND connection inserted? |  |
| Is DRC along with dummy fill Report **clean?** |  |
| Is Antenna along with dummy fill Report **clean?** |  |
| Dummy Fill done |  |
| Grid size **0.005µm** used for layout |  |
| Whether Pads connected till **top metal (TOP\_M) ?** |  |
| Final Chip Origin should be at (0,0) after seal ring insertion. |  |
| Process Information Sheet duly filled? |  |

1. **Reports to be included** (please **√** on the following if provided)

|  |  |
| --- | --- |
| Final DRC run Reports (Result database including density logs, summary, transcript, runset version) |  |
| Final Antenna Report (Result database, summary, transcript, runset version) |  |
| Devices type (or legal devices) used in layout report |  |
| Stream out log files |  |
| List of third party IP used (If any with prior approval from SCL) |  |
| List of SCL IP used (If any with prior approval from SCL) |  |
| List of all legal layers used before silicon number insertion in Excel Format  (Layer Name + layer number + datatype) |  |
| Coordinate of Silicon number |  |
| Process Information Sheet (Attached PIS Excel) |  |

Note: Prior to final submission of GDSII please contact ChipIN Team for insertion of Silicon Number Structure in layout at your end. Silicon Number will be generated by SCL PDK Team as per SCL Numbering System through ChipIN Centre. Contact Emails for obtaining Silicon Number: [chipin@cdac.in](mailto:chipin@cdac.in).

1. **Guidelines/ Notes for packaging**
   1. Bonding diagram also shall be submitted along with the design submission for fabrication.
   2. Followings need to be ensured by ChipIN center during the submission of any GDSII to SCL
      * The bonding diagram has been generated and verified
      * All the packaging related data/files based on the final bonding diagram must be submitted in the final data pack

|  |  |  |
| --- | --- | --- |
| **Tape-out and Packaging related Checklist** | | **Please Tick / Specify** |
| Mention the Die size including seal ring. Options supported: **2 x 2 mm2,3 x 3 mm2 , 4 x 4 mm2  or 5 x 5 mm2**  *(No other size is supported in the current tapeout under this program) For sizes greater than 5 x 5* **mm 2** *ChipIN will contact SCL’s PPG.* | | Specify **2 x 2 mm2 or 3 x 3 mm2 or 4 x 4 mm2 or 5 x 5 mm2** |
| The design should have a seal ring around it. The distance between chip boundary to seal ring should be minimum of 10um with DRC Clean | |  |
| The seal ring is connected to VSS (Ground) | |  |
| No. of pins for Packaging the IC  *(Currently no. of pins should not be more than 100 for packaging)* | | Specify the No. of Pins |
| Package selected for packaging (Refer Appendix – I) | Specify the Package Serial Number |  |
| The minimum pitch between two adjacent bond pads is 90um for all bond pads | |  |

**Any other Remarks from Designer/Reviewer:**

**Name and Signature of the Designer Name and Signature of the Reviewer/Approving Authority**

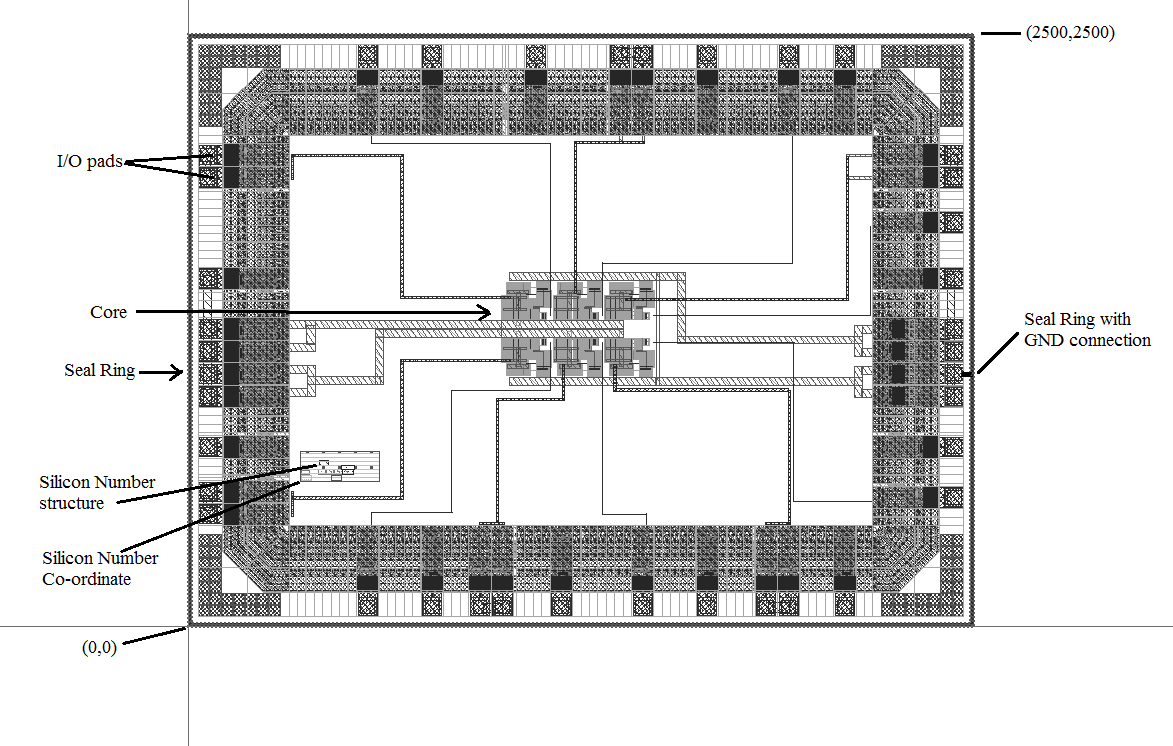
(PI / Co-PI of the Institution)

Date and Seal:

**APPENDIX - I**

**Preferred Die Size and plastic packages (Chip-on-Board<CoB> Packaging Options)**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Sr. No.** | **Die Size (mm)** | **Package Size (mm)** | **Pin Count** | **Package Lead Pitch (mm)** | **CoB Package Type** |
| 1 | 2.0 x 2.0 | 7.0 x 7.0 | 16 | 1.0 | QFN |
| 2 | 3.0 x 3.0 | 7.0 x 7.0 | 16 | 1.0 | QFN |
| 3 | 2.0 x 2.0 | 8.4 x 8.4 | 24 | 1.0 | QFN |
| 4 | 3.0 x 3.0 | 8.4 x 8.4 | 24 | 1.0 | QFN |
| 5 | 3.0 x 3.0 | 9.0 x 9.0 | 28 | 1.0 | QFN |
| 6 | 2.0 x 2.0 | 10.0 x 10.0 | 32 | 1.0 | QFN |
| 7 | 3.0 x 3.0 | 10.0 x 10.0 | 32 | 1.0 | QFN |
| 8 | 2.0 x 2.0 | 14.0 x 14.0 | 48 | 1.0 | QFN |
| 9 | 3.0 x 3.0 | 14.0 x 14.0 | 48 | 1.0 | QFN |
| 10 | 2.0 x 2.0 | 18.0 x 18.0 | 64 | 1.0 | QFN |
| 11 | 3.0 x 3.0 | 18.0 x 18.0 | 64 | 1.0 | QFN |
| 12 | 4.0 x 4.0 | 14.0 x 14.0 | 48 | 1.0 | QFN |
| 13 | 5.0 x 5.0 | 14.0 x 14.0 | 48 | 1.0 | QFN |
| 14 | 4.0 x 4.0 | 18.0 x 18.0 | 64 | 1.0 | QFN |
| 15 | 5.0 x 5.0 | 18.0 x 18.0 | 64 | 1.0 | QFN |
| 16 | 4.0 x 4.0 | 10.0 x10.0 | 72 | 1.0 | QFN |
| 17 | 5.0 x 5.0 | 20.0 x 20.0 | 72 | 1.0 | QFN |
| 18 | 4.0 x 4.0 | 20.0 x 20.0 | 80 | 1.0 | QFN |
| 19 | 5.0 x 5.0 | 20.0 x 20.0 | 80 | 1.0 | QFN |
| 20 | 4.0 x 4.0 | 25.0 x 25.0 | 88 | 1.0 | QFN |
| 21 | 5.0 x 5.0 | 25.0 x 25.0 | 88 | 1.0 | QFN |
| 22 | 4.0 x 4.0 | 28.0 x 28.0 | 100 | 1.0 | QFN |
| 23 | 5.0 x 5.0 | 28.0 x 28.0 | 100 | 1.0 | QFN |

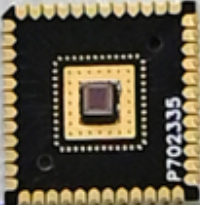
****Example Design:**

**Example package:**

A diagram of a square with lines and numbers

Description automatically generated

|  |  |
| --- | --- |
| **Label Name** | **Indicators** |
| a | Package Size |
| b | Die Attach Pad Size |
| c | Package Lead Pitch |



QFN Type CoB Package